Reduced Layer Planar Busbar for Voltage Source Inverters

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***Abstract*—Planar busbars are used widely in modern high power inverters and have been shown to provide a good way for minimizing stray inductance and overshoot voltage. Planar busbars, which consist of multilayer copper sheets and dielectric insulators, offer significant advantages such as low impedance, improved thermal characteristic and reduced system cost compared with other interconnection approaches. A common problem of hard switched inverters is stray inductance, which needs to be minimized to reduce the effect of over voltages. This paper presents a new physical structure for a voltage source inverter with symmetrical planar busbar structure, which minimizes the variation in stray inductance for different switching states. Three-dimensional (3-D) finite element simulations and experimental tests verify the theory.**

***Index Terms*—Inductance, planar busbar, voltage source inverter.**

I. Introduction

IN POWER electronic circuits, such as an inverter, the interconnection inductance between the dc supply and inverter components can be a major problem using point to point wiring. The reduction of the wiring inductance is an important issue in high power and fast switching inverters. This is a common issue for all conventional hard switched converters and the stray inductance should be kept as low as possible to minimize over voltages. Using large area thin conductor sheets with rectangular cross section separated by dielectric sheets (planar busbar) instead of circular cross section wires, contributes to a reduction of the stray inductance. Thus, the use of the planar busbar is highly desirable for high power inverters when fast hard switching is employed.

The calculation for the inductance and the resistance of conductors at low and high frequencies has been examined by [2], [3], [6], [9], and [11]. He compared two kinds of conductors, rectangular and circular cross section bars. This results show that the rectangular busbar is the preferred shape to minimize the stray inductance. A number of approximate equations exist for calculating the inductance of a rectangular conductor [5], [8], [12]. However, exact equations have been derived for the inductance between a parallel filament and rectangular bars in [7]. In deriving the equations given in these papers, the assumption was made that the current density was uniform throughout the conductors, which is not valid for an inverter with a current point injection.

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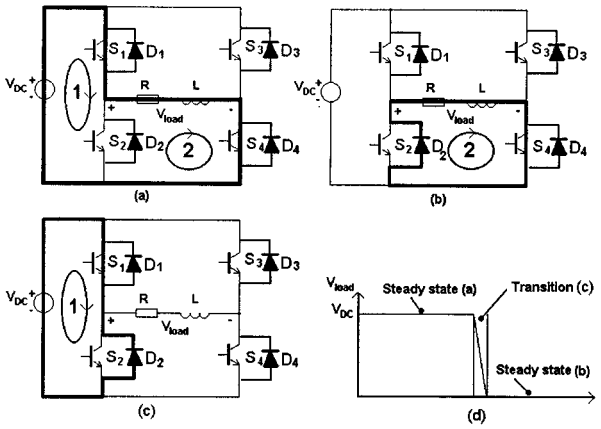

Fig. 1. Current loops at different times for (a) $V_{\rm load} = V_{\rm dc}$, (b) $V_{\rm load} = 0$, (c) transition time, and (d) output voltage across the load.

A mathematical analysis of the planar busbar has been performed at low and high frequencies in [10] and determined the inductance and the resistance values between two points of the planar busbar. This paper then draws on the theory of [10] to present a new physical structure for the planar busbar called reduced layer planar busbar. The new voltage source inverter with symmetrical planar busbar structure minimizes the variation in stray inductance for different switching states. Three-dimensional (3-D) finite element simulations and experimental tests verify the theory.

II. Current Loops in a Voltage Source Inverter

In an inverter circuit, a dc voltage source is connected to the power electronic switches and a load through busbars and produces the desired output voltage using the pulse width modulation technique (PWM). For example, Fig. 1(a) shows the case where the voltage across the load is $V_{\rm load} = V_{\rm DC}$, and also defines two load current loops. When the switch state changes such that the load voltage is zero, $(V_{\rm load} = 0)$, the load current now only passes through the second loop as shown in Fig. 1(b). During the switching time, Fig. 1(c), the current loop around loop 1 must go to zero. As soon as S_1 starts to turn off, D_2 turns fully on (the load current does not change due to the inductive load). Since D_2 is conducting, the following equation is satisfied around loop1 at the transition time:

$$V_{S1} = V_{\rm DC} - L_1 \frac{di}{dt} \tag{1}$$

where L_1 is the total stray inductance of loop 1 and V_{S1} is the voltage across switch S_1. Thus, while S_1 is turning off the stray

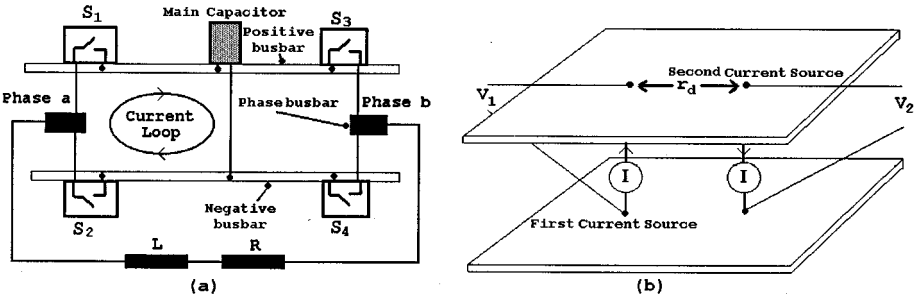

Fig. 2. (a) Cross section of a planar busbar used for a single phase inverter and (b) current loop associated with Fig. 2(a).

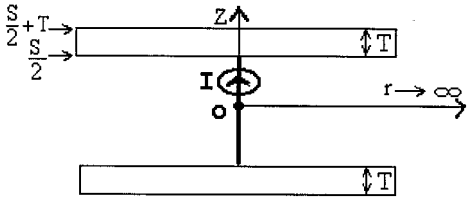

Fig. 3. Cross section of a planar busbar with one current source at the origin.

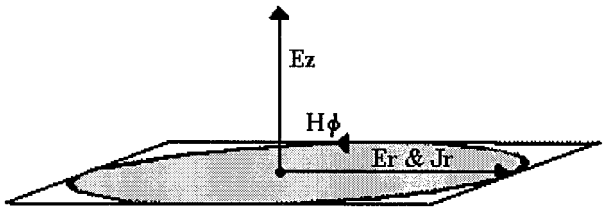

Fig. 4. Field vectors in cylindrical coordinates.

inductance of the loop will cause an over voltage across switch S_1 based on (1).

To minimize the over voltage across the switch, the stray inductance of the current loop must be kept as low as possible. The use of the planar busbar is highly desirable for high power inverters when fast and hard switching is employed. Fig. 2(a) shows a cross section of a planar busbar used for a single phase voltage source inverter. The current loop passes through switches S_1 and S_2, the main capacitor and the busbars as shown in the circuit diagram of in Fig. 1(c). To calculate the impedance of the planar busbar, two current sources are connected to the planar busbar at the location of the main capacitor and the switches, S_1 & S_2 as shown in Fig. 2(b). Thus, the objective is to find the loop inductance of Fig. 2(b) in terms of sheet separation, distance between the current sources and other parameters such as conductivity and permeability.

III. Busbar Analysis

A mathematical analysis of the planar busbar has been performed at low and high frequencies in [10] and determined the inductance and the resistance values between two points of the planar busbar. In [10], two parallel sheets (planar busbar) are considered using cylindrical coordinates and two sinusoidal current sources of the form $Ie^{(j\omega t)}$ are applied with polarities as shown in Fig. 2(b). It is assumed that both conductors have the same finite thickness, T, and finite separation, S. For the analysis in [10], the first current source which is located at the origin is applied in order to determine the magnetic and electric fields as shown in Fig. 3. The effect of the second current source at the location of $r = r_d$ is considered using superposition as shown in Fig. 2(b).

It is assumed that only vector components J_r, H_ϕ, E_z and E_r exist due to the symmetrical situation in cylindrical coordinates as shown in Fig. 4.

The r and z variations of the field vectors can be determined using Maxwell's equations

$$\nabla \times (\nabla \times \vec{E}) = -\frac{\partial}{\partial t}(\nabla \times \vec{B}). \tag{2}$$

This yields

$$\nabla^2 \vec{E} = \mu \frac{\partial}{\partial t}\left(\sigma \vec{E} + \varepsilon \frac{\partial \vec{E}}{\partial t}\right). \tag{3}$$

Since we have assumed sinusoidal time variation, (3) becomes

$$\nabla^2 \vec{E} = (j\omega\mu\sigma - \omega^2\mu\varepsilon)\vec{E}. \tag{4}$$

The problem is to find H_ϕ, E_z and E_r in terms of constants which are evaluated using the boundary conditions.

First consider the dielectric region where conductivity, $\sigma \cong 0$. Thus, (4) becomes

$$\nabla^2 \vec{E} = \omega^2 \mu\varepsilon \vec{E}. \tag{5}$$

Since $H_\phi = 0$, then (5) reduces to the r and z components as follows:

$$\left(\nabla^2 E_r - \frac{E_r}{r^2}\right)\vec{a}_r + \nabla^2 E_z \vec{a}_z = -\omega^2\mu\varepsilon(E_r\vec{a}_r + E_z\vec{a}_z). \tag{6}$$

If a solution of the form $E_r(r,z) = R(r)Z(z)$ is assumed, (6) becomes

$$\frac{1}{R}\frac{\partial^2 R}{\partial r^2} + \frac{1}{rR}\frac{\partial R}{\partial r} - \frac{1}{r^2} = -\frac{1}{Z}\frac{\partial^2 Z}{\partial z^2} - \omega^2\mu\varepsilon = -b^2 \tag{7}$$

where b is a constant value. Thus, E_r becomes

$$E_r = CN_1(br)\mathrm{Sin}(a_1 z) \tag{8}$$

where $a_1^2 = \omega^2\mu\varepsilon - b^2$, $N_1(br)$ is known as a Bessel function of first order [1].

The constants C, b, and a_1 are determined using boundary conditions.

Since there is only a φ component of H, Maxwell's equation gives

$$\nabla \times \vec{H} = \left(-\frac{\partial H_\varphi}{\partial z}\right)\vec{a}_r + \left[\frac{1}{r}\frac{\partial (rH_\varphi)}{\partial r}\right]\vec{a}_z = j\omega\varepsilon\vec{E}. \tag{9}$$

The two separated equations are

$$-\frac{\partial H_\varphi}{\partial z} = j\omega\varepsilon E_r \tag{10}$$

$$\frac{1}{r}\frac{\partial (rH_\varphi)}{\partial r} = j\omega\varepsilon E_z. \tag{11}$$

Using (8) and (10), H_ϕ can be expressed as

$$H_\varphi = \frac{jC\omega\varepsilon}{a_1} N_1(br)\mathrm{Cos}(a_1 z). \tag{12}$$

Then E_z can be found by using (11) and (12) as

$$E_z = \frac{Cb}{a_1} N_o(br)\mathrm{Cos}(a_1 z) \tag{13}$$

where $N_o(br)$ is a Bessel function of order zero [1].

Now consider the conductor region. It is assumed that the displacement current is negligible compared to the conduction current and that E_z is equal to zero in the conductor region. Since $\omega^2\mu\varepsilon \ll \omega\mu\sigma$, (4) gives

$$\nabla^2\vec{E} = j\omega\mu\sigma\vec{E}. \tag{14}$$

The vector fields H_ϕ and E_r in the conductor region can be found in a similar fashion to that applied in the dielectric region.

Thus, E_r and H_ϕ become

$$E_r = N_1(br)\left[C_1 e^{-a_2 z} + C_2 e^{a_2 z}\right] \tag{15}$$

$$H_\varphi = \frac{\sigma N_1(br)}{a_2}\left[C_1 e^{-a_2 z} - C_2 e^{a_2 z}\right] \tag{16}$$

where $a_2^2 = b^2 + j\omega\mu\sigma$, C_1 and C_2 are constants.

In the last section, the field vectors were found in the dielectric and the conductor regions. The constant values from the last equations can be determined using the boundary conditions. At the dielectric-conductor boundary, $z = (S/2)$, the tangential components of E_r and H_ϕ must be equal as shown in Fig. 3. Thus

$$(E_{r_{(\mathrm{Conductor})}} = E_{r_{(\mathrm{Dielectric})}})|_{z=S/2} \tag{17}$$

$$(H_{\varphi_{(\mathrm{Conductor})}} = H_{\varphi_{(\mathrm{Dielectric})}})|_{z=S/2}. \tag{18}$$

It is assumed that the busbar dimension is large in "r" direction, then the magnetic field, H_ϕ, is contained between the conductors but is negligible on outside of the busbars. Thus

$$H_{\varphi_{(\mathrm{Conductor})}} = 0|_{z=(S/2)+T}. \tag{19}$$

The final boundary condition is related to the current source connections to the busbars. As shown in Fig. 3, the current source is connected to the busbar by a round conductor with radius r_o. Thus, the value of the current can be defined as

$$I = \int J\cdot ds = \sigma\int E\cdot ds. \tag{20}$$

Expressing this surface integral using cylindrical coordinates

$$I = \sigma\iint E_r\cdot(2\pi r_o d\varphi dz) = 2\pi r_o\sigma\int_{(S/2)}^{(S/2)+T} E_r\cdot dz. \tag{21}$$

A simple way to calculate busbar impedance is using Ohm's law. Thus, the voltage values across the current sources can be found using $V = \int_{-(S/2)}^{+(S/2)} E_z\cdot dz$. Therefore

$$V_1 = \frac{jISbN_o(br_o)}{2\pi r_o\omega\varepsilon N_1(br_o)} \tag{22}$$

where

a_2 $(1+j)\sqrt{\pi f\mu\sigma}$;
a_1 $\sqrt{(j2\omega\varepsilon a_2\coth(a_2T))/\sigma S}$;
b $\sqrt{\omega^2\varepsilon\mu - a_1^2}$;
ω $2\pi f$;
f frequency;
μ permeability;
ε permittivity;
σ conductivity;
T thickness of sheet;
S separation between sheets.

The voltage value at the location of the second current source $(r = r_d)$ due to the first current source is

$$V_2 = \frac{jISbN_o(br_d)}{2\pi r_o\omega\varepsilon N_1(br_o)}. \tag{23}$$

The voltage value across the busbar due to the first current source becomes

$$V_1 - V_2 = \frac{jISbN_o(br_o)}{2\pi r_o\omega\varepsilon N_1(br_o)} - \frac{jISbN_o(br_d)}{2\pi r_o\omega\varepsilon N_1(br_o)}. \tag{24}$$

The voltage value due to the second current source can be calculated using symmetry and is the same as found in (24). Using superposition law, the total voltage value due to the first and second current sources becomes

$$V_{\mathrm{eq}} = 2(V_1 - V_2). \tag{25}$$

Thus, the input impedance of the busbar associated with Fig. 2(b) can be expressed as follows:

$$Z = R + j\omega L = \frac{V_{\mathrm{eq}}}{I}. \tag{26}$$

IV. Physical Location of Components

The reduction of the stray inductance is an important issue in high power and fast switching inverters to minimize transient over voltages. It has been proven that the planar busbar has a lower inductance value than other types of interconnections [8], [11], [12].

In Section III, the inductance of the planar busbar was found in terms of the distance between the current injection points, separation between the conductive sheets and other parameters such as conductivity and permeability. The planar busbar structure for the inverter consists of copper sheets and electrical insulators with known conductivity and permeability. The next alternative method to minimize stray inductance is to investigate the effect of physical location of the power electronic components and the planar busbars in order to minimize the distance between the current injection points (current sources) and the busbar separation.

A. Physical Location of a Main Capacitor

Fig. 5 shows a cross section of a planar busbar used for a single phase voltage source inverter with dc bus capacitor, C. Two current loops, Loop_1 and Loop_2, with different lengths are shown in Fig. 5(a) corresponding to different transition times. Because the performance is limited by the worst possible case, the inductance of the second loop, Loop_2, has to be minimized for optimization.

Clearly, the stray inductance of Loop_2 can be optimized when the main capacitor, C, is located between the phase legs due to the symmetrical loop paths as shown in Fig. 5(b). Thus, it is crucial to consider the location of the main capacitor and other components in order to minimize the loop inductance length in addition to optimising the physical structure of the busbar.

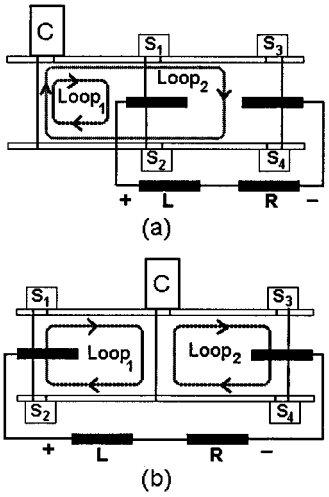

Fig. 5. Current loops at the transition times for different locations of the main capacitor (a) at the side and (b) at the center.

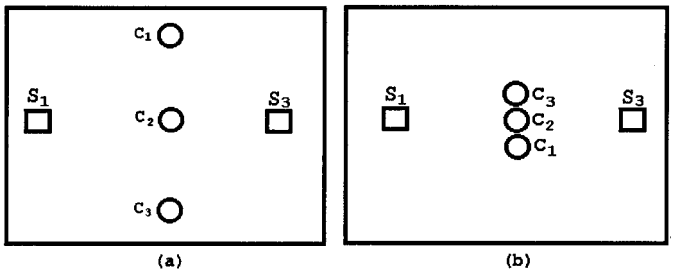

Fig. 6. Top view of the planar busbar with (a) distributed capacitors and (b) concentrated capacitors.

B. Distributed Capacitors

In high power inverters, the dc bus voltage source typically consists of several capacitors in parallel in order to provide a low ripple dc voltage during operation. The capacitors can be installed in a concentrated form or distributed over the busbar surface as shown in Fig. 6. During switching, the current loop under transition occurs between the capacitors and the power electronic switches. It is expected that the planar busbar with the distributed capacitors has a lower inductance value compared to the concentrated form, as the current through the busbar becomes more uniformly distributed.

To examine the effect of capacitor location on busbar inductance we use the current source approach as performed in [10]. Using (22)–(26) which were derived in Section III, the impedance of the planar busbar with distributed capacitors can be found by considering three current sources at the location of the three capacitors as shown in Fig. 7. The current source at the location of OO' is returned via three current sources, where $I = I_1 + I_2 + I_3$. Thus, the voltage values at the locations of the other current sources due to one of the current sources can be evaluated out using (22). The total impedance of the planar busbar with three capacitors is not simply a matter of computing three independent impedances between each loop using (26). Instead, the voltages at points OO', A_1B_1, A_2B_2 and A_3B_3 due to each current source need to be determined using (22) in order to find the self and the mutual impedances. Using superposition, the total voltage across each current source location due to the different current sources has been taken into the account. The

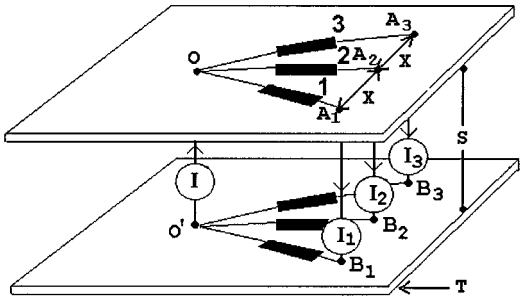

Fig. 7. Current loops of the planar busbar with three capacitors.

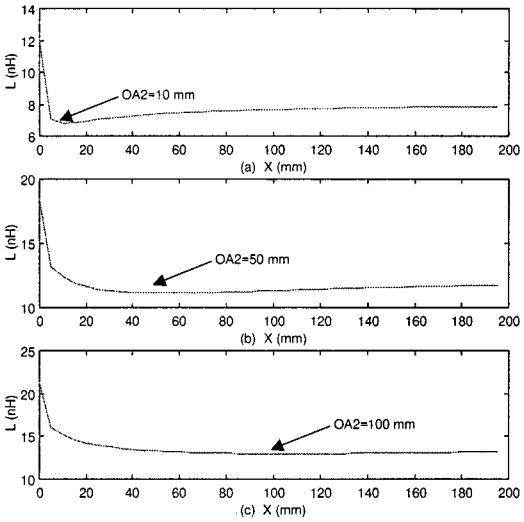

Fig. 8. Inductance values of the planar busbar with three capacitors as a function of capacitor separation X.

self and the mutual impedances of the planar busbar with three current loops can be defined as follows:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ Z_{31} & Z_{32} & Z_{33} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \tag{27}$$

where the V_k is the voltage across the kth current source and $Z_{\rm ij}$ is the mutual impedance between loop ith and jth.

To simplify the impedance equation, it is assumed that $OA_1 = OA_3 = r_d$, $OA_2 = r_b$ and $A_1A_2 = A_2A_3 = X$ as shown in Fig. 7. The total impedance of the planar busbar with three capacitors can be expressed as follows:

$$Z_{\rm eq} = \frac{V_{\rm in}}{I_{\rm in}} = \frac{V_{\rm in}}{I_1 + I_2 + I_3}. \tag{28}$$

Using (22)–(27), $Z_{\rm eq}$ becomes

$$Z_{\rm eq} = \frac{jSbK_1}{2\pi\omega r_o \mu_o N_1(br_o) K_2} \tag{29}$$

where

$$\begin{aligned} K_1 =& 4N_o(br_o)^2 - 2N_o(br_d)^2 - 2N_o(br_b)^2 - 2N_o(bx)^2 \\ &+ 4N_o(br_o)[N_o(br_d) + N_o(bx)] \\ &+ 4N_o(br_d)[N_o(br_b) + N_o(bx)] \\ &+ 2N_o(2bx)[N_o(br_o) - N_o(br_b)] \\ &+ 2N(2br_b)[2N_o(bx) - N_o(br_o)] \\ K2 =& 3N_o(br_o) - 4N_o(bx) + N_o(2bx). \end{aligned}$$

Fig. 8 shows the inductance values of the planar busbar with three connections in terms of the separation between the capac-

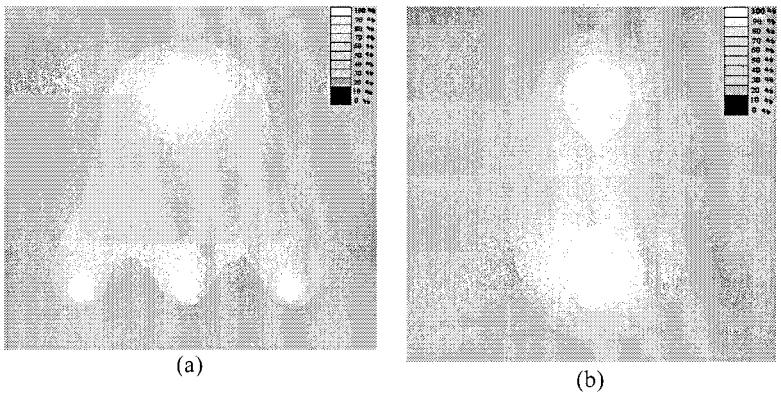

Fig. 9. Current density for (a) three connections associated with Fig. 7 and (b) single connection associated with Fig. 2(b).

itors, X, for $OA_2 = 10$, 50, 100 mm ($T = 1$ mm, $S = 10$ mm, $f = 1$ MHz). When X approaches to zero, the two current sources at the location of A_1 and A_3 move to the location of A_2 and the planar busbar with three connections becomes to the planar busbar with one connection. For $X = 0$, the inductance value of the planar busbar from (29) becomes the same as the one from (26). For example, Fig. 8(a) shows the inductance value of the planar busbar with three connections in terms of the separation between the capacitors, X, for $OA_2 = 10$ mm. At $X = 0$, the inductance value is approximately 12 nH using (29) and it is equal to the inductance value of the planar busbar with one connection using (26).

When A_1 and A_3 are further from A_2 (separation between capacitors, X, is increased) the current through the busbar becomes more uniformly distributed and the inductance value is improved due to the lower current density. The minimum inductance value occurs when $A_1A_2 = A_2A_3 = OA_2$. The separation between capacitors, X, can not be increased more than OA_2 in order to decrease the inductance value of the planar busbar. Because the loop impedances, Z_1 and Z_3 are increased and the current is not shared well between the loops. Then, most of the current passes through Z_2 and the effects of the other impedances, Z_1 and Z_3 are reduced.

C. Simulation Results

Three-dimensional finite element field software, Ansoft [13] has been utilized to confirm the analytical results. The package includes electrostatic, nonlinear magnetic, current conduction and eddy current analysis. These tools provide computation of device parameters such as force, torque, saturation effect, inductance, capacitance and power losses. There is no intrinsic limit to the size of the problem. The simulator can be commanded to make high-density meshes inside the busbar and the insulator in order to increase the accuracy of the simulation. As the mesh size increased, more memory and multi-processors are required for the simulation.

Simulations at various frequencies have been carried out for a copper planar busbar with three connections as shown by Fig. 7. The busbars have been separated by an air insulator with ($T = 1$ mm; $S = 10$ mm; $r_b = 50$ mm; $X = 50$ mm; dimension of the busbars 20×20 cm). The background around the modeled planar busbar has been defined large enough (20 times of the modeled busbar) to avoid boundary effects of the simulator solution. As the modeled busbar consists of parallel sheets, Cartesian coordinate were used to draw the busbar and the results (field vectors) can be transferred and shown in an alternative coordinate system. The field simulation is performed using an ac current source including skin and proximity effects and the simulation software automatically computes the impedance and the inductance of the modeled busbar.

TABLE I
THEORY AND SIMULATION RESULTS OF PLANAR BUSBAR IMPEDANCE AT DIFFERENT FREQUENCIES

Frequency	1 MHz	2 MHz	3 MHz
$L_{Simulation}$	13.74 nH	13.6nH	13.46 nH
L_{Theory}	11.28 nH	11.09 nH	11.08 nH
$R_{Simulation}$	.525 mil-Ohm	.701 mil-Ohm	.801 mil-Ohm
R_{Theory}	.458 mil-Ohm	.647 mil-Ohm	.794 mil-Ohm

Fig. 9 shows the current density through the planar busbar with three and one connections. From the simulator tools, a plane surface is defined in the planar busbar along the sheet to show the data in 2 dimensions. Fig. 9(a) shows that the current through the busbar with three connections have been distributed more than the one connection as shown in Fig. 9(b). Clearly a planar busbar with multiple connections exhibits a lower inductance due to better current distribution.

Table I shows the simulation and theory results of the planar busbar with three connections (with the above dimensions) at various frequencies. There are differences between the theory and simulation results which are associated with the dimensions of the planar busbars and feasible limits on mesh size. In the theory, it was assumed that the planar busbar has a very large surface area, while in the simulation, the dimensions are finite.

As shown in Fig. 10, the major effect is to decrease the dimension of the busbar along the x direction, while reduction the busbar width in the y direction is less significant in causing an increase in the planar busbar inductance. If the dimension of the planar busbar in the y direction, "b," is bigger than 1.5 times of r_d, the simulation results show the effect of the busbar

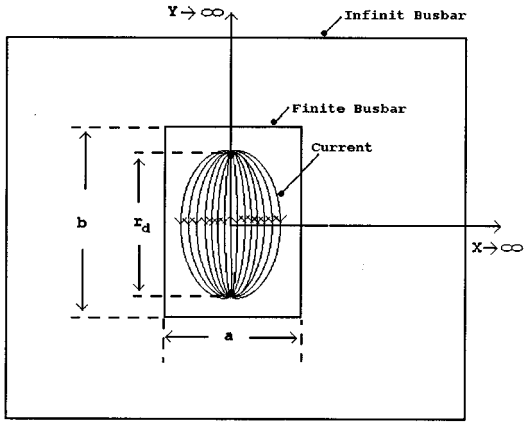

Fig. 10. Top view of a finite and infinite planar busbars.

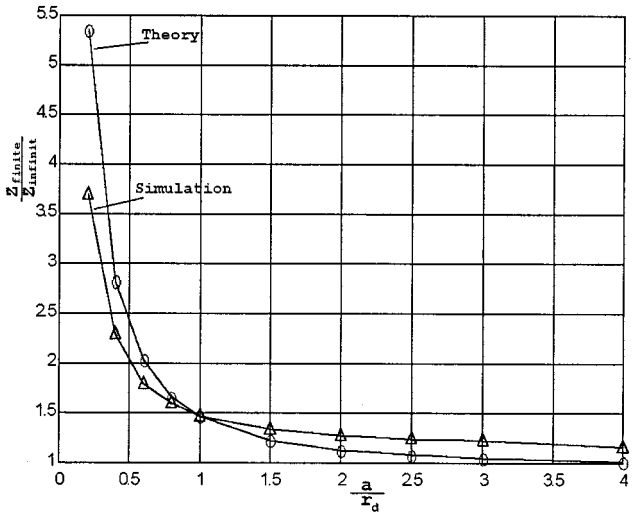

Fig. 11. Theory and simulation results of finite planar busbar impedance in terms of a/r_d.

dimension will be negligible along the y direction. Considering the total current which passes through the finite busbar should influence the geometry used in the calculation. The impedance of the finite busbar in terms of the ratio of the busbar side in the x direction, "a," to the distance between the current sources, r_d, has been calculated by theory using the current density through the finite busbar and it was compared with simulation results.

For a planar busbar with, $(a/r_d) \geq 4$, the theoretical results can be used to find the busbar impedance with error less than 10%, while for $(a/r_d) \leq 4$, the impedance ratio, $Z_{\text{finite}}/Z_{\text{infinit}}$ has to be calculated using Fig. 11 for the impedance of the planar busbar. As shown in Fig. 11, the inductance value of the finite planar busbar is linearly decreased from 1.35 down to 1.2 times of the inductance value of the infinite planar busbar when a/r_d ratio is increased from 1.5 up to 4, respectively. At $a/r_d = 4$, the inductance value is not significantly decreased while the size, cost and weight of the planar busbar structure are increased. Also, when the ratio is decreased to less than 1, the inductance value increases nonlinearly and the busbar form is changed to a strip form losing the advantages of the planar busbar. Thus, for commercial proposes, the size of the planar busbar for high power applications is recommended in the range $1 \leq a/r_d \leq 1.5$.

V. Reduced Layer Planar Busbar

In Sections II–IV, it has been shown that the inductance of the planar busbar is a Bessel function of the separation between injection points, while the inductance value is proportionally related to the separation between the busbars, S. Examine the two cases in Fig. 12, decreasing the separation between the busbars, S, and increasing the separation between the injection points, r_b, by a factor of 2.

Using (24)–(26), doubling the separation between the busbars, S, increases the inductance by 2 times while doubling the separation between the injection points, r_b, increases L, 1.12 times. Therefore, the inductance value of the planar busbar with the structure shown in Fig. 12(a) is 1.78 times of the other one in Fig. 12(b). Thus, the separation between the busbars is the major factor which has to be kept as low as possible consistent with insulation requirements.

In a single phase inverter shown in Fig. 2, the transition current loops occur between the main capacitors, the switches (S_1 and S_2 or S_3 and S_4) and the planar busbars at transition times. These current loops show that the separation between the positive and the negative busbars is very important to minimize the stray inductance. The separation between these busbars, which carry the loop current, is $2T_{\text{Insulator}} + T_{\text{Conductor}}$ where $T_{\text{Insulator}}$ and $T_{\text{Conductor}}$ are the thicknesses of the insulator and the conductor, respectively. Therefore, changing the location of each layer of the planar busbar is an option to decrease the separation between the positive and the negative busbars and thus to minimize the stray inductance.

Figs. 8 and 9 show that the planar busbar with distributed capacitors has a lower inductance value compared to the concentrated form (one connection) due to a better current distribution in the busbars. This concept leads to the proposed new structure of planar busbar (reduced layer planar busbar) for power electronic inverters with a very low stray inductance and allowing better airflow for thermal cooling as shown in Fig. 13. In this new structure, the positive and the negative busbars, which are connected to the dc supply, are side-by-side on the top of the phase busbars. At the transition time, the current loops occur between the upper busbars, which are connected by the main capacitors and the phase busbar. The inductance value of the reduced layer planar busbar is much less than the other one shown in Fig. 2 since the separation between busbars has decreased to $T_{\text{Insulator}}$. Assuming the upper busbars of the reduced layer inverter is a single sheet of Copper. Then, Figs. 2(a) and 13(a) can be associated with Fig. 12(a) and (b), respectively. In the reduced layer planar busbar, for the upper busbars the conduction across the busbar is via capacitors rather than conductor connections. Thus, an equation for the inductance value of the reduced layer planar busbar is a new objective, which has to be investigated.

Three-dimensional finite element simulations have been performed for the reduced layer planar busbar with different connections. The busbars have been separated by an air insulator with ($T = 1$ mm; $S = 10$ mm; $r_b = 80$ cm; $X = 15$ cm; dimension of the busbars 120×60 cm). Simulation results show that the inductance value of the planar busbar with one, three and five connections are 1.49, 1.13, 1.07 times that of the planar busbar with infinite connections (uniform sheet).

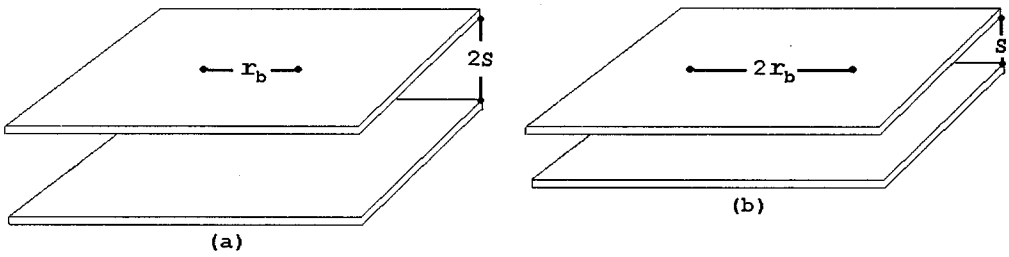

Fig. 12. Physical structures of planar busbar: (a) double separation between busbars and (b) double separation between injection points.

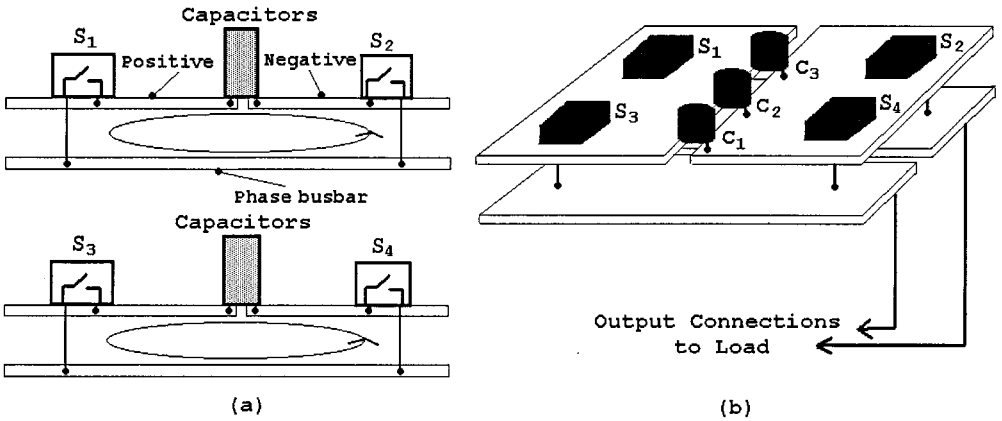

Fig. 13. Reduced layer planar busbar for inverter: (a) current loop at transition times and (b) physical structure.

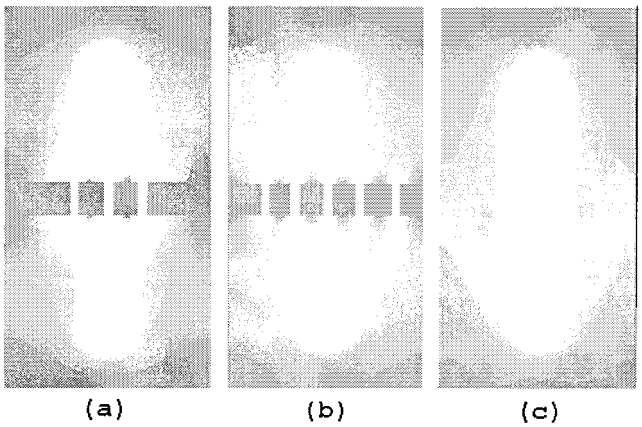

Fig. 14. Simulation results of the current distribution through the busbar for various connections: (a) three, (b) five, and (c) uniform sheet.

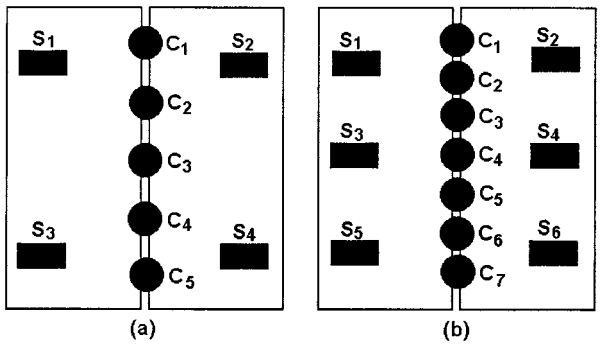

Fig. 15. Top view of the planar busbar: (a) five capacitors for a single phase inverter and (b) seven capacitors for a three phase inverter.

As the number of the capacitors are increased, the current distribution through the busbar approaches that of the uniform sheet busbar as shown in Fig. 14(c). If the number of the capacitors is high enough to produce a good current density similar to Fig. 14(a) or (b), the approximate impedance value can be derived using (24) since the current distribution through the busbar is very close to the uniform planar busbar as shown in Fig. 14(c).

Thus, the reduced layer planar busbar is recommended for high power inverters when the number of capacitors is more than $(2p+1)$ where p is a number of phases. For example, in a single phase inverter, the first current loop occurs between the power electronic switches S_1 and S_2 and the five capacitors where at least three of them (C_1 and C_2 and C_3) pass most of the current as shown in Fig. 15(a). In this case, at least three capacitors carry the loop current during switching time and the current distribution through the busbar is close to the uniform planar busbar shown in Fig. 14. The three phase case is shown in Fig. 15(b).

VI. Thermal Considerations

Heat is generated when current passes through the busbars due to ohmic losses. Heat transfer occurs by convection, conduction and radiation from the hot material (busbar) to the ambient. Thermal resistance is associated with the conduction or convection of heat. Thus, the thermal resistances for conduction and convection are related to the surface area, thickness, conduction and convection conductivities. The total thermal resistance can be found by adding the conduction and convection resistances [4]. The planar busbars may consist of different layers of busbars and electric insulators with series and parallel thermal resistances due to implicit structures. The thermal resistance has to be decreased as low as possible to transfer the heat

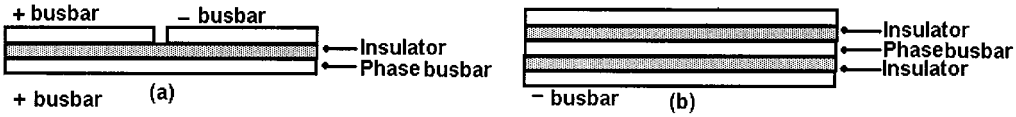

Fig. 16. Physical structure of planar busbars: (a) reduced layer and (b) parallel.

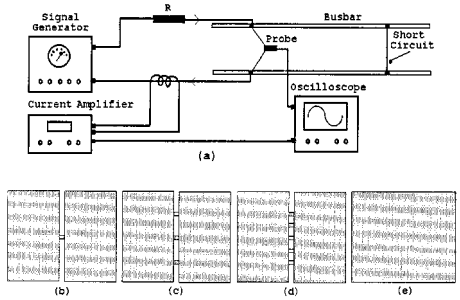

Fig. 17. (a) Circuit diagram for experiment test on a planar busbar, upper busbars with: (b) single connection, (c) three connections, (d) five connections, and (e) uniform sheet.

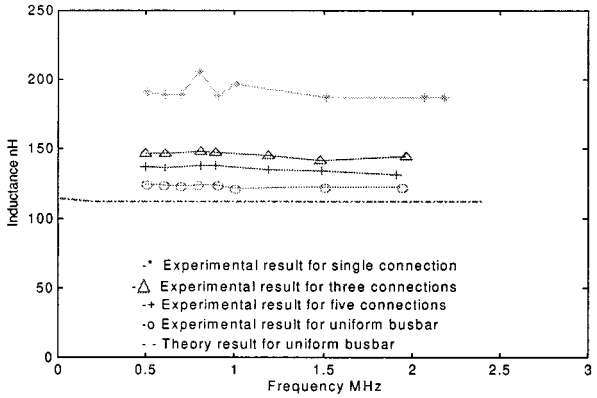

Fig. 18. Inductance value of the side-by-side planar busbar with various connections.

from different layers of the busbars. Fig. 16 shows two different structures of the planar busbars, reduced layer and parallel. One of the advantages of the reduced layer planar busbar is that all busbars have one side to transfer the heat to the ambient directly as shown in Fig. 16(a), while the internal busbar of the parallel structure has to transfer the heat through the insulators and the busbars with a high thermal resistance.

VII. Experimental Results

To validate the theory results, experimental tests have been performed to determined the inductance values of the planar busbar at various frequencies. For experimental tests, the reduced layer planar busbar consists of two copper sheets ($T = 1$ mm; $r_b = 80$ cm, $X = 10$ cm, dimension of the busbars 120×60 cm) joined by some strip conductors on the top of the uniform sheet separated by an air insulator as shown in Fig. 17. During switching time, transition current loops occur between the switches, capacitors and busbars. To measure the inductance value of the busbar, a sinusoidal current is injected into one point of the busbar and at the another point a short circuit is made as a returning path. Indeed, as shown in Fig. 17, the strip wires connected to the upper busbars and the short circuit are related to the current paths through the capacitors and the power electronic switch at transition times, respectively.

A signal generator injects a sinusoidal current with $I = 200$ mA, into the reduced layer planar busbar and a voltage across the injection points has been measured. For low inductance values such as 10 nH, V_{in} becomes approximately 6 mV at 100 kHz, which is difficult to measure. To increase the voltage across the injection points, V_{in}, the inductance of the planar busbar has been increased in order to have an accurate measurement. Thus, the separation between the busbars is changed to $S = 4$ cm in this experimental test to validate the theory. It should be noted that in power electronic applications the inductance of the planar busbar has to be kept as low as possible using lower separations.

The reduced layer planar busbar with four different types of connections has been examined. Experimental results show that the inductance value of the planar busbar with three and five connections are very close to the uniform sheet as shown in Fig. 18.

The inductance value of the reduced layer planar busbar with one connection between the upper busbars is much higher than three or more connections. Therefore, the new structure of the planar busbar is recommended for high power inverters, if the number of the main capacitors is more than five or seven for single phase or three phase inverters, respectively.

VIII. Conclusions

A reduced layer planar busbar has been presented in this paper as a new structure of busbar for high power inverters with minimum separation between busbars, optimum stray inductance and improved thermal performances. This type of the planar busbar is suitable for high power inverters, where the voltage source consists of some capacitors in parallel in order to provide a low ripple dc voltage during operation. To calculate the point-input impedance of the planar busbar with distributed capacitors, mathematical analysis has been performed based on Maxwell's equations. The inductance value of the reduced layer planar busbar is minimized by decreasing the separation between busbars, which carry the transition current. The location of the power electronic components and the physical location of each layer have been shown to be important for minimizing the loop inductance The minimum separation between busbars is limited by the dielectric strength. The distance between the switch and dc source depends on the physical dimensions of device and dc line capacitors.

Another common problem in the conductors is the thermal energy generated from passing a current through the busbar. The wide and thin planar busbars without any internal busbars are

preferable for heat dissipation from the busbar surface due to a better air contact with each conductor.

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